library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity adder is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC;

carry : out STD\_LOGIC);

end adder;

architecture Behavioral of adder is

begin

sum<=a xor b;

carry<=a and b;

end Behavioral; LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric\_std.ALL;

ENTITY addertest IS

END addertest;

ARCHITECTURE behavior OF addertest IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT adder

PORT(

a : IN std\_logic;

b : IN std\_logic;

sum : OUT std\_logic;

carry : OUT std\_logic

);

END COMPONENT;

--Inputs

signal a : std\_logic := '0';

signal b : std\_logic := '0';

--Outputs

signal sum : std\_logic;

signal carry : std\_logic;

-- No clocks detected in port list. Replace <clock> below with

-- appropriate port name

-- constant <clock>\_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: adder PORT MAP (

a => a,

b => b,

sum => sum,

carry => carry

);

-- Clock process definitions

--<clock>\_process :process

--begin

--<clock> <= '0';

--wait for <clock>\_period/2;

--<clock> <= '1';

--wait for <clock>\_period/2;

-- end process;

-- Stimulus process

stim\_proc: process

begin

-- hold reset state for 100 ns.

a<='0';

b<='0';

wait for 100 ns;

a<='0';

b<='1';

wait for 100 ns;

a<='1';

b<='0';

wait for 100 ns;

a<='1';

b<='1';

wait for 100 ns;

--wait for <clock>\_period\*10;

-- insert stimulus here

wait;

end process;

END;

